

Claims:

1. A magnetic random access memory (MRAM) device,
5 comprising:

an array of magnetic memory cells that store
data as different values of impedance;

a grid of bit and word lines for selectively
accessing data in the array of magnetic memory cells; and

10 a plurality of diodes, each connected in series
with a respective ones of said magnetic memory cells and
between corresponding ones of the grid of bit and word
lines;

wherein, the number of bit and word lines
15 possible in the grid is increased by the inclusion of the
plurality of diodes that reduce leakage currents
circulating through non-selected ones of the magnetic
memory cells.

20 2. The MRAM of claim 1, wherein a distribution of
data-write currents in the grid associated with different
ones of said magnetic memory cells across the array varies
less than 15% in operation.

25 3. A magnetic random access memory (MRAM) device,
comprising:

an array of magnetic memory cells that store
data as different values of impedance;

a grid of bit and word lines for selectively
30 accessing data in the array of magnetic memory cells; and

a plurality of diodes, each connected in series
with a respective ones of said magnetic memory cells and

between corresponding ones of the grid of bit and word lines;

wherein, the operating margin for each memory cell is increased by the inclusion of the plurality of
5 diodes that reduce leakage currents circulating through non-selected ones of the magnetic memory cells.

4. A method for making MRAM devices, comprising:
electrically isolating each and every memory
10 cell in an MRAM array during operation until selected, wherein, a more uniform distribution of read and data-write data access currents on selected bit and word lines results to all said memory cells; and
increasing the number of rows and columns to
15 support a larger data array.

5. A method for making MRAM devices, comprising:
electrically isolating each and every memory
cell in an MRAM array during operation until selected,
20 wherein, a more uniform distribution of read and data-write data access currents on selected bit and word lines results to all said memory cells; and
increasing operating margins to reduce minimum data-write voltages and currents.